

**METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A  
CAPACITOR AND A RESISTOR**

**FIELD OF THE INVENTION**

The present invention relates generally to semiconductor fabrication and more specifically to simultaneous formation of capacitors, resistors and metal-oxide semiconductors.

## **BACKGROUND OF THE INVENTION**

Analog integrated circuits may include active elements such as metal-oxide semiconductors and passive elements such as capacitors and resistors formed on a semiconductor substrate and interconnected by wiring patterns.

U.S. Patent No. 6,246,084 B1 to Kim describes a method for fabricating a capacitor and resistor over a shallow trench isolation (STI) structure.

U.S. Patent No. 5,618,749 to Takahashi et al. describes another method for fabricating a capacitor and resistor over a shallow trench isolation (STI) structure.

U.S. Patent No. 5,434,098 to Chang describes a capacitor process with an interpoly oxide (IPO) layer.

U.S. Patent No. 5,656,524 to Eklund et al. describes a method of forming a polysilicon resistor.

## **SUMMARY OF THE INVENTION**

Accordingly, it is an object of one or more embodiments of the present invention to provide improved methods of simultaneously forming a capacitor(s) and resistor(s) on a field oxide film and a metal-oxide semiconductor(s) on a semiconductor substrate.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having: an exposed oxide structure; a capacitor region within at least a portion of the exposed oxide structure; a first resistor region within at least a portion of the exposed oxide structure; a second resistor region within at least a portion of the exposed oxide structure; and a metal-oxide semiconductor region not within at least a portion of the exposed oxide structure is provided. A first polysilicon layer is formed over the structure and the exposed oxide structure. The first polysilicon layer is doped to form a doped first polysilicon layer. An interpoly oxide film is formed over the doped first polysilicon layer. The interpoly oxide film is patterned to form: a capacitor interpoly oxide film portion within the capacitor region over the oxide structure; and a second interpoly oxide film portion within the second resistor region over the oxide structure. A second polysilicon layer is formed over the structure. The second polysilicon layer is doped to form a doped second polysilicon layer. The doped second polysilicon layer and the doped first

polysilicon layer are patterned to form: within the capacitor region: a lower capacitor doped first polysilicon portion underneath at least a portion of the capacitor interpoly oxide film portion, and an overlying upper capacitor second doped polysilicon portion over at least a portion of the patterned capacitor interpoly oxide film portion; within the first resistor region: a lower first resistor first polysilicon portion and an upper, overlying first resistor second polysilicon portion; within the second resistor region: a lower second resistor first polysilicon portion underneath at least a portion of the second interpoly oxide film portion; and within the metal-oxide semiconductor region: a lower metal-oxide semiconductor first polysilicon portion and an overlying metal-oxide semiconductor second polysilicon portion.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 4 schematically illustrate a preferred embodiment of the present invention.

## **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

### **Initial Structure – Fig. 1**

As shown in Fig. 1, structure 70 includes an exposed oxide structure 78 formed therein. Structure 70 includes a capacitor region 72 including at least a portion of the oxide structure 78, a first resistor region 74 including at least a portion of the oxide structure 78, a second resistor region 75 including at least a portion of the oxide structure 78 and a metal-oxide semiconductor (MOS) region 76 that does not include a portion of the oxide structure 78.

Oxide structure 78 is preferably a field oxide (FOX) film having a thickness of preferably from about 4000 to 7500Å and more preferably from about 4000 to 5500Å.

Structure 70 is preferably a silicon (Si), germanium (Ge) or gallium arsenide (GaAs) substrate, is more preferably a silicon substrate.

A first polysilicon layer 80 is formed over structure 70 and exposed oxide structure 78 to a thickness of preferably from about 1000 to 2500Å and more preferably from about 1500 to 2000Å. The first polysilicon layer 80 is then doped, preferably with phosphorus (P) or arsenic (As) and more preferably with

phosphorus (P) to a concentration of preferably from about  $1\text{E}16$  to  $1\text{E}21$  atoms/cm<sup>2</sup> and more preferably from about  $1\text{E}18$  to  $1\text{E}20$  atoms/cm<sup>2</sup>.

An interpoly oxide (IPO) film 86 is formed over the doped first polysilicon layer 80 to a thickness of preferably from about 250 to 600Å and more preferably from about 300 to 450Å.

#### Patterning of IPO Film 86 - Fig. 2

As shown in Fig. 2, the IPO film 86 is patterned to form:

a capacitor IPO film portion 86' within the capacitor region 72 over the oxide structure 78; and

a second IPO film portion 87' within the second resistor region 75 over the oxide structure 78.

#### Formation of Second Polysilicon Layer 89 – Fig. 3

As shown in Fig. 3, a second polysilicon layer 89 is formed over first doped polysilicon layer 80 and IPO film portions 86', 87' to a thickness of preferably from about 1000 to 2500Å and more preferably from about 1500 to 2000Å. The second polysilicon layer 89 is then doped, preferably with phosphorus (P) or arsenic (As) and more preferably with phosphorus (P) to a concentration of preferably from about  $1\text{E}19$  to  $1\text{E}21$  atoms/cm<sup>2</sup> and more preferably from about  $5\text{E}19$  to  $5\text{E}20$  atoms/cm<sup>2</sup>.

Patterning of Second Doped Polysilicon Layer 89 and First Doped Polysilicon Layer 80 – Fig. 4

As shown in Fig. 4, the second doped polysilicon layer 89 and first doped polysilicon layer 80 are patterned to form:

within capacitor region 72: a lower capacitor doped first polysilicon portion 82 underneath at least a portion of capacitor IPO film portion 86', and an overlying upper capacitor second doped polysilicon portion 88' over at least a portion of the patterned capacitor IPO film portion 86';

within first resistor region 74: a lower first resistor first polysilicon portion 90 and an upper, overlying first resistor second polysilicon portion 94;

within second resistor region 75: a lower second resistor first polysilicon portion 94 underneath at least a portion of second IPO film portion 87'; and

within MOS region 76: a lower MOS first polysilicon portion 84 and an overlying MOS second polysilicon portion 96 that comprise a MOS electrode 97.

It is noted that one or more capacitors and/or MOSs; and two or more resistors may be formed in accordance with the teachings of the third embodiment of the present invention.

Further processing may then proceed.

### Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. the total thickness of the first polysilicon and second polysilicon is thinner than prior art, it can increase process throughput and save process cost;
2. the thickness of first polysilicon is thinner, so the topography is plainer than prior art, it is helpful to photo process due to the wider photo DOF window;
3. it is easy to integrate polycide module, we can use polycide (e.g. WSi) film to replace second polysilicon, and then we can implement a polycide gate process; and
4. there are two kinds of resistors, one is formed by first polysilicon, and the other one is formed by the combination of first and second polysilicon.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.